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Lesson 103 - Example 70: Block RAM

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the SiSoft Quantum Channel Designer User Guide (provided with the SIS Kit installation). Page 8: Installation And Requirements

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2, 2008 09/11/07 3.1 Chapter 1: Added  
“ Clock Gating for Power Savings ” on  
page 22 . Revised Figure 1-2, page 26 .

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Revised Figure 1-16, page 33. Chapter 2:  
Revised DCM reset and locking process in  
“ Reset Input - RST, ” page 49 .

Updated DO[2] description in Table 2-4,  
page 52.

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remains below this voltage. (This  
parameter is basically the hysteresis for  
logic ' 0 ' .) VIH(max) must not exceed  
1.9V for all Micron Parts. [www.xilinx.com](http://www.xilinx.com)  
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ROMs) with one output, or as two 5-input LUTs (32-bit ROMs) with separate outputs but common addresses or logic inputs. Four such LUTs and four flip flops as well as multiplexers and arithmetic carry logic form a slice, and two slices form a Configurable Logic Block (CLB).



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